the second region;

an offset region of the second conductivity type formed selectively in the surface portion of the first region between the second region and the third region;

a first insulation film on the offset region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the offset region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other.

2. (Amended) The semiconductor device according to Claim 1, wherein the depths of the sub-regions of the [second] offset region are different from each other.--

--4. (Amended) A semiconductor device exhibiting a high breakdown voltage, the semiconductor device comprising:

a semiconductor substrate of a second conductivity type;

a first region of a first conductivity type formed selectively in the surface portion of the semiconductor substrate;

a second region of the second conductivity type formed selectively in the surface portion of the semiconductor substrate;

a third region of the first conductivity type formed selectively in the surface portion of the first region;

the second region and the third region being spaced apart from each other;

a fourth region of the first conductivity type formed selectively in the surface portion of the second region;

an offset region of the second conductivity type formed selectively in the surface portion

of the first region between the second region and the third region;

a first insulation film on the offset region;

a gate electrode above the extended portion of the second region extending between the fourth region and the first region with a gate insulation film interposed between the extended portion of the second region and the gate electrode;

a first main electrode on the fourth region; and

a second main electrode on the third region;

wherein the offset region comprises a plurality of sub-regions aligned between the second region and the third region, the impurity concentrations of the sub-regions being different from each other.

5. (Amended) The semiconductor device according to Claim 4, wherein the depths of the sub-regions of the offset region are different from each other.--

--13. (Amended) The semiconductor device according to Claim 1, wherein the surface impurity concentration of the offset region of the second conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof being less than the amount of the impurity of the second conductivity type in the offset region.

14. (Amended) The semiconductor device according to Claim 4, wherein the surface impurity concentration of the offset region of the second conductivity type is changed by adding an impurity of the first conductivity type, the amount thereof being less than the amount of the impurity of the second conductivity type in the offset region.--